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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,916	07/09/2001	Simon Tam	110031	4508

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EXAMINER	
LIANG, REGINA	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/899,916	TAM, SIMON	
	Examiner	Art Unit	
	Regina Liang	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-58* is/are allowed.

6)☒ Claim(s) *62,64 and 72-75* is/are rejected.

7)☒ Claim(s) *59-61, 63, 65-71* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

2. Claims 69, 70 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda (US. PAT. NO. 5,714,968).

As to claim 69, Fig. 9 of Ikeda teaches a driving method to drive a driving circuit for a current driven element (1), comprising a first step for setting a first operating voltage of a first transistor (17) and a second operating voltage of a second transistor (16) by flowing a data current to a data signal, and a second step for supplying a driving current to the current driven element through the first transistor and the second transistor (col. 8, line 16 to col. 9, line 16).

As to claim 70, Ikeda teaches in the first step, the first and second transistors (16, 17) act as diodes (the current flows in one direction).

Claim Rejections - 35 USC § 103

3. Claims 59-61, 63, 65-68, 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda.

As to claim 59, Ikeda does not disclose the first transistor being an n-channel transistor, the second transistor being a p-channel transistor. However, Ikeda suggests that the first and second transistor can be an n-channel transistor, a p-channel transistor or a bipolar junction transistor (col. 9, lines 8-16). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the first transistor and the second transistor of Ikeda to be a n-channel transistor and a p-channel transistor as claimed so as to provide a drive

circuit which is capable of driving the current dependent element with a reduced current and voltage.

As to claims 60, 61, Fig. 9 of Ikeda teaches the driver circuit having a first storage capacitor and a second storage capacitor (18, 19), and the first storage capacitor (19) being disposed between a first source (9) and the first gate of the first transistor (17), the second storage capacitor (18) being disposed between a second source (9) and the second gate of the second transistor (16).

As to claim 63, Fig. 9 of Ikeda teaches a switching device (14, 15) controlling electrical connection between the current source of the data current (3) and one of the first and second transistors.

As to claim 65, Fig. 9 of Ikeda teaches a switching device (14, 15) controlling electrical connection between the first source (12) and first gate (17), and controlling electrical connection between the second source (130 and the second gate (16).

As to claim 66, Ikeda teaches the transistor comprising polysilicon TFT (col. 10, lines 26-28).

As to claim 67, Ikeda teaches the current driven element (1) being an EL element.

As to claim 68, Fig. 9 of Ikeda shows the first and the second transistor being disposed in close proximity to each other.

As to claim 71, Ikeda teaches an electro-optical device comprising the driver circuit.

Allowable Subject Matter

4. Claims 35-58 are allowed.

5. Claims 62, 64, 72-75 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 7/14/04 have been fully considered but they are not persuasive.

Applicant's remarks regarding Ikeda on page 10 are not persuasive. Ikeda, in Fig. 9 and col. 8, lines 16 to col. 9, line 16, discloses when the voltages on the first data line 12 and the second data line 13 are both 0V, no current flowing through the transistors 16 and 17 (since the gate voltage of both transistors are 0V, so the both transistors 16 and 17 are turned off, no current flows through the transistors 16 and17). When the voltage of the data line 12 becomes 5V, the current of about $2x10^{-1}$ (mA) flows through the transistor 17 (since the gate voltage of transistor 17 is sufficient to turn on the transistor 17, so the current flows through the transistor 17 and to the EL element 1), and when the voltage of the data line 13 becomes 5V, the current of about $2x10^{-1}$ (mA) flows through the transistor 16 (since the gate voltage of transistor 16 is sufficient to turn on the transistor 16, so the current flows through the transistor 16 and to the EL element 1), which reads on setting a first operating voltage of a first transistor and a second operating voltage of a second transistor by flowing a data current according to a data signal, and supplying a driving current to the current driven element through the first transistor and the second transistor as recited in claim 69.

In response to applicant's argument on page 11 that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or

modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Ikeda suggests that the first and second transistor can be an n-channel transistor, a p-channel transistor or a bipolar junction transistor (col. 9, lines 8-16).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (703) 305-4719. The examiner can normally be reached on Monday-Friday from 9AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

REGINA LIANG
PRIMARY EXAMINER
ART UNIT 2674

RL
10/29/04